UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,922	06/27/2003	Meng-Huang Liu	COR 127	3859

23995 7590 07/26/2004

RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,922	LIU ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8 and 11-27* is/are rejected.

7)☒ Claim(s) *6,7,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 3, 5, and 15 are objected to because of the following informalities:

In regards to claim 3, the limitation "said first region is from a semiconductor substrate" is objected to. It is suggested the term "from" be removed.

In regards to claims 5 and 15, there is insufficient antecedent basis for "said input pad". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, 11, 14, and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US Pat. 6,258,634, hereinafter Wang).

In regards to claim 1, Figure 3 of Wang discloses an ESD protection apparatus comprising: a first region (P-Substrate) of a first conductivity type; a second region 116 of a second conductivity type opposite to said first region; a third region 116 of said first conductivity type formed in said second region; a first input connection region 122 of said first conductivity type and a second input connection region 112 of said second conductivity type both formed in said third region; and a first ground connection region 124 of said first conductivity type and a second ground connection region 120 of said second conductivity type both formed on said first

region. It is inherent that the output (cathode K) of an ESD device be connected to ground at some point in order to discharge the excess current. Therefore, regions 120 and 124 can be considered ground connection regions.

In regards to claim 2, Figure 3 of Wang discloses a bridge region of said second conductivity type across said second region and extending to said first and third regions. Note that a portion of region 116 near the surface, between region 114 and the P-substrate, can be considered the bridge region.

In regards to claim 3, Figure 3 of Wang discloses the first region (p-substrate) is from a semiconductor substrate.

In regards to claim 4, Figure 3 of Wang discloses said first, second, and third regions (p-substrate, 116, and 114, respectively) are arranged in a triple well manner.

In regards to claim 5, it is inherent that the first and second input connection regions (122 and 112) are connected to some type of input pad at some point in the electronic device, and that said first and second ground connections (124 and 120) are connected to a some type of ground pad at some point in the electronic device.

In regards to claim 8, the intended use limitation "wherein said first, second, and third regions form two back-to-back diodes under a normal operation" does not structurally distinguish the claimed invention over Wang. Figure 3 of Wang discloses alternating p-n-p semiconductor regions; therefore it is capable of forming back-to-back diodes.

In regards to claim 11, Figure 3 of Wang discloses an ESD apparatus comprising: an SCR structure 100 including a first and a second semiconductor regions (P-substrate and 114, respectively) of a first conductivity type inserted with a third semiconductor region 116 of a

second conductivity type opposite to said first conductivity type therebetween; a first electrode region 124/120 connected to said first semiconductor region, said first electrode region having a first part 124 of said first conductivity type and a second part 120 of a said second conductivity type; and a second electrode region 122/112 connected to said second semiconductor region, said second electrode region having a first part 122 of said first conductivity type and a second part 112 of said second conductivity type.

In regards to claim 14, the limitation "wherein said SCR structure is formed by CMOS triple-well process" is a product-by-process limitation that does not structurally distinguish the claimed invention over Wang.

In regards to claim 19, Figure 3 of Wang discloses an ESD protection method comprising the steps of: forming a first and second semiconductor regions (114 and P-substrate, respectively) of a first conductivity type inserted with a third semiconductor region 116 of a second conductivity type opposite to said first conductivity type therebetween; forming a first electrode region 122/112 connected to said first semiconductor region, said first electrode region having a first part 122 of said first conductivity type and a second part 112 of a said second conductivity type; and a second electrode region 124/120 connected to said second semiconductor region, said second electrode region having a first part 124 of said first conductivity type and a second part 120 of said second conductivity type. It is inherent that the output of an ESD device be connected to ground at some point in order to discharge the excess current. It is also inherent that the first electrode region is connected to some type of input pad at some point in the electronic device, and that the second electrode region is connected to some type of ground pad at some point in the electronic device.

In regards to claim 20, Figure 3 of Wang discloses the first, second, and third semiconductor regions (114, P-substrate, and 116, respectively) are formed by CMOS triple well process.

In regards to claim 21, Figure 3 of Wang discloses a bridge region of said second conductivity type across said third region 116 and extending to said first and third regions. Note that a portion of region 116 near the surface, between region 114 and the P-substrate, can be considered the bridge region.

Claims 11-20 and 22-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang. The following rejections are based on an alternate interpretation of the Wang reference.

In regards to claim 11, Figures 3 and 5 of Wang discloses an ESD apparatus comprising: an SCR structure 100 including a first and a second semiconductor regions (118 and 114, respectively) of a first conductivity type inserted with a third semiconductor region 116 of a second conductivity type opposite to said first conductivity type therebetween; a first electrode region 124/120 connected to said first semiconductor region, said first electrode region having a first part 124 of said first conductivity type and a second part 120 of a said second conductivity type; and a second electrode region 122/112 connected to said second semiconductor region, said second electrode region having a first part 122 of said first conductivity type and a second part 112 of said second conductivity type.

In regards to claim 12, Figure 5 of Wang discloses a PN junction 126 breaking down to said first semiconductor region 118 under a positive polarity ESD event (col. 5, lines 38-47).

In regards to claim 13, it is inherent that a PN junction 128 will break down to said second semiconductor region 114 under a negative ESD event since the process will simply be reversed.

In regards to claim 14, the limitation "wherein said SCR structure is formed by CMOS triple-well process" is a product-by-process limitation that does not structurally distinguish the claimed invention over Wang.

In regards to claim 15, Figure 5 of Wang discloses the first and second parts (124 and 120) of the first electrode region 118 are connected to a ground pad, and said first and second parts (122 and 112) of said second electrode region 114 are connected to said input pad A. It is inherent that the output (cathode K) of an ESD device be connected to ground at some point in order to discharge the excess current.

In regards to claims 16 and 17, Figure 5 of Wang discloses said first and second parts of the first and second electrode regions (124, 120, 122, and 112, respectively), as well the first, second and third semiconductor regions (118, 114, and 116, respectively) all together for an SCR circuit under a positive polarity ESD event. This also holds true for a negative ESD event since the operation of the device is simply reversed.

In regards to claim 18, the intended use limitation "wherein said first semiconductor region, third semiconductor region, and second semiconductor region form two back-to-back diodes under a normal operation" does not structurally distinguish the claimed invention over Wang. Figure 5 of Wang discloses alternating p-n-p semiconductor regions; therefore it is capable of forming back-to-back diodes.

In regards to claim 19, Figures 3 and 5 of Wang disclose an ESD protection method comprising the steps of: forming a first and second semiconductor regions (114 and 118, respectively) of a first conductivity type inserted with a third semiconductor region 116 of a second conductivity type opposite to said first conductivity type therebetween; forming a first electrode region 122/112 connected to said first semiconductor region, said first electrode region having a first part 122 of said first conductivity type and a second part 112 of a said second conductivity type; and a second electrode region 124/120 connected to said second semiconductor region, said second electrode region having a first part 124 of said first conductivity type and a second part 120 of said second conductivity type. It is inherent that the output of an ESD device be connected to ground at some point in order to discharge the excess current. It is also inherent that the first electrode region is connected to some type of input pad at some point in the electronic device, and that the second electrode region is connected to some type of ground pad at some point in the electronic device.

In regards to claims 20 and 25, Wang discloses forming the semiconductor regions by a CMOS process (col. 4, lines 35-37). Since the device of Figure 3 has three wells, it is considered Wang forms the device by a CMOS triple-well process.

In regards to claims 22, 23, 26, and 27, Wang discloses forcing a junction breakdown at said second semiconductor region 118 under a positive polarity ESD event (col. 5, lines 38-47). It is inherent that a PN junction 128 will break down to said first semiconductor region 114 under a negative ESD event since the process will simply be reversed.

In regards to claim 24, Figure 5 of Wang discloses an ESD protection method comprising the steps of: forming an SCR structure; connecting a first electrode region 122/112 having

regions of opposite conductivity types to said SCR structure; connecting a second electrode region 124/120 having regions of opposite conductivity types to said SCR structure; connecting said first electrode region to said input pad A; and connecting said second electrode region to a ground pad. It is inherent that the output of an ESD device be connected to ground at some point in order to discharge the excess current.

Claim 24 is rejected under 35 U.S.C. 102(b) as being anticipated by Rountre (US Pat. 5,012,317).

In regards to claim 24, Figures 2b and 3 of Rountre disclose an ESD protection method comprising the steps of: forming an SCR structure; connecting a first electrode region 48/50 having regions of opposite conductivity types to said SCR structure; connecting a second electrode region 52/54 having regions of opposite conductivity types to said SCR structure; connecting said first electrode region to said input pad 12; and connecting said second electrode region to a ground pad.

In regards to claim 26, Rountre discloses forcing a junction breakdown (avalanche) to lower a triggering voltage of said SCR structure under a positive polarity ESD event (col. 5, lines 13-17).

Allowable Subject Matter

Claims 6, 7, 9 and 10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claim 6, the prior art of record, either singularly or in combination, does not disclose or suggest said first input connection region, third region, second region, first region, and first and second ground connections region form an SCR circuit under a positive polarity ESD event.

In regards to claim 7, the prior art of record, either singularly or in combination, does not disclose or suggest said first and second input connection regions, third region, second region, first region, and first ground connection region form an SCR circuit under a negative polarity ESD event.

In regards to claim 9, the prior art of record, either singularly or in combination, does not disclose or suggest said bridge region breaks down to said first region under a positive polarity ESD event.

In regards to claim 10, the prior art of record, either singularly or in combination, does not disclose or suggest said bridge region breaks down to said third region under a negative polarity ESD event.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or

proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Matthew C. Landau

Examiner

July 24, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800